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09/181,253	10/28/1998	GREGORY MICHAEL KAROL	98004	9665

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EXAMINER	
KUMAR, PANKAJ	
ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 10/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/181,253	Applicant(s) KAROL, GREGORY MICHAEL	
	Examiner Pankaj Kumar	Art Unit 2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. DETAILED ACTION

2. Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

4. The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 1 recites the limitation "said PLL filter circuit" in page 14 line 2. Claim 14 also recites this limitation. There is insufficient antecedent basis for this limitation in the claims.

7. Claims 1 and 14 recite the limitation "an input coupled to said multiplexer output and a frequency output". This limitation is reciting one input with "an input" but then defines two inputs – a multiplexer output input and a frequency output input.

8. Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

10. A person shall be entitled to a patent unless –

11. (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
12. (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

13. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined

was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

14. Claims 1-4, 7, 10-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Bedrosian USPN 5740211.

15. As per claim 1, a clock circuit comprising: first (Bedrosian fig. 9A: side 0 monitor output) and second clock sources (Bedrosian fig. 9A: side 1 monitor output); a multiplexer having a first input (Bedrosian fig. 9A: CLK MUX top input) coupled to the first clock source, a second input (Bedrosian fig. 9A: CLK MUX bottom input) coupled to the second clock source (Bedrosian col. 4 fourth paragraph "(12) The hitless switch device 130 has an input multiplexer 202 which is connected to clock distribution circuits 120, 121 and is capable of receiving a side 0 set of clock and sync signals, and a side 1 set of clock and sync signals therefrom. Input multiplexer 202 selects between these sets of clock and sync signals from sides 0 or side 1. The switching selection is controlled either by input failure monitors or by a manual command (not shown)."), and an output selectively couplable to said first and second inputs (Bedrosian fig. 9A: bottom output of CLK MUX into flip flop in which one of the inputs is a select into the D input of the flip flop); a clock detection circuit having an output representing a presence of said first clock source (Bedrosian fig. 9A: bottom NOR gate); said multiplexer having a selection input coupled to said clock detection circuit output (Bedrosian fig. 9A: NOR gate coupled to CLK MUX via flip flop) such that said multiplexer selects said first clock source as its output when

said first clock source is present (Bedrosian fig. 9A: system will force 0 or force 1 depending on whether 0 or 1 is present); a phase-locked loop circuit ("PLL") (Bedrosian fig. 9B) having an input coupled to said multiplexer output (Bedrosian fig. 9A output from CLK MUX goes into fig. 9B top input) and a frequency output (Bedrosian fig. 9A output from SYNC MUX goes into fig. 9B bottom input), said PLL including a feedback filter circuit (Bedrosian fig. 9B: LPF 2nd order); and feedforward circuitry (Bedrosian fig. 9B: number of locations for example – top input going through latch, inverter and AND gate circuits in order to reach phase compare circuit while top input also going through middle and bottom latches which eventually affect the D latch towards the middle left of the diagram whose output is eventually fed into the phase comparator) coupled to said feedback filter circuit (Bedrosian fig. 9B: phase comparator is coupled to LPF) and coupled to said clock detection circuit output (Bedrosian fig. 9B: latches 0011, 0100, and two 0001 are clock enabled and thus they are detecting clocks), said feedforward circuitry selectively coupling at least one circuit element to said PLL filter circuit (rejected under 112), wherein said selective coupling is controlled by said clock detection circuit output.

16. As per claim 2, the circuit of claim 1, where said feedforward circuitry includes a switch controlled by said clock detection circuit output and performing said selective coupling (Bedrosian fig. 9B: the second input into the ET phase compare whose output eventually goes into the LPF is derived via a clock through the AND gate inputting into the ET phase compare. AND gate is working as a switch since its output will only switch high when both of its inputs are switched high. Selective coupling is occurring since the clock is selected (select 0/1) prior to these steps).

17. As per claim 3, the circuit of claim 2, wherein said switch comprises a transistor (Bedrosian fig. 9A: inherent for the flip flop to have transistors).

18. As per claim 4, the circuit of claim 2, wherein said at least one circuit element includes a resistor (Bedrosian fig. 2: 206 "pulse blocker").

19. As per claim 7, the circuit of claim 2, further including a bias circuit coupling said clock detection circuit output to said switch (Bedrosian fig. 9B: the D latch towards the middle left of the diagram is the bias circuit coupling the clock output to the AND gate which is essentially functioning as a switch).

20. As per claim 10, the circuit of claim 1, wherein said first clock source (Bedrosian fig. 9A: Side 0) is received from another clock circuit within a common system (Bedrosian fig. 9A: received by monitor for clk mux as well as monitor for sync mux).

21. As per claim 11, the circuit of claim 10, wherein said first clock source is received over a bus. (Bedrosian fig. 9A: inputs into monitors are indicated as buses since a width of 2 is indicated for the inputs to the monitors)

22. As per claim 12, the circuit of claim 11, wherein said second clock source comprises a local oscillator. (inherent for a clock source to comprise a local oscillator since a clock source is itself oscillating)

23. As per claim 13, the circuit of claim 12, wherein said second clock source (Bedrosian fig. 9A: Side 1) is provided to said bus (Bedrosian fig. 9A: inputs into the monitor is indicated as a bus since a width of 2 is indicated).

24. As per claim 14, a system comprising: multiple clock sources; a switch having multiple inputs, said multiple inputs being respectively coupled to said multiple clock sources; a clock detection circuit having an output representing a presence of one of said multiple clock sources; said switch having a selection input coupled to said clock detection circuit output such that said switch selects one particular clock source of said multiple clock sources as its output when said one particular clock source is present; a phase-locked loop circuit ("PLL") having an input coupled to said switch output and a frequency output, said PLL including a feedback filter circuit; and feedforward circuitry coupled to said feedback filter circuit and to said clock detection circuit output, said feedforward circuitry selectively coupling at least one circuit element to said PLL filter circuit, wherein said selective coupling is controlled by said clock detection circuit output. (discussed in claim 1)

25. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Fazakerly et al. USPN 4208635.

26. As per claim 15, a circuit comprising: a clock source (Fazakerly fig. 1: reference frequency) ; a PLL circuit having said clock source as its input (Fazakerly fig. 1: 10, 12, 14); a detection circuit coupled to said clock source (Fazakerly fig. 1: 10) and having an output responsive to a presence of said clock source (Fazakerly fig. 1: 10 is responsive to its input); and a feedforward correction circuit (Fazakerly fig. 2: 34, 36) coupled to said output of said detection circuit (Fazakerly fig. 2: Vout) and to a feedback loop of said PLL (Fazakerly fig. 2: 46, 51; col. 3 line 50 to col. 4 line 12).

27. Claims 16-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Richards et al. USPN 6178207.

28. As per claim 16, a method for controlling a clocking circuit including a clock source coupled to an input of a phase-locked loop ("PLL") circuit comprising: detecting a failure of said clock source; applying a control signal to said PLL in response to said failure of said clock source, said control signal altering a time constant within said PLL. (Richards paragraphs 59 and 63: "The gain starts at one for the first transition of a message, and drops as each additional bit change occurs following a 1/(N+1) sequence, where N is the number of transitions since the start of the message. To accommodate clock drift during long stretches without data transitions, the gain increases with each bit period (with or without a data transition) by a factor of 2.sup.-m (1-G), where m is the user determined factor that sets the time constant J of the filter and G is the instantaneous tracking loop gain ... If the time constant J of the filter circuit 1208 is zero (m=0),

then the circuit takes the new clock transition value as the new clock signal timing (that is, the correction factor is 100%). Therefore, in the case of J=0, it doesn't matter how recently the most recent transition (and therefore clock information) was received, the new transition is taken as valid and the clock out signal is fixed to the new transition. Those skilled in the art will recognize that this operation is different from that of a conventional phase lock loop, which takes some fixed portion of old and new data to set a new frequency. In this way, the clock recovery circuit 1208 of the invention provides an adaptive PLL.")

29. As per claim 17, the method of claim 16, wherein said altering said time constant includes modifying a feedback loop (Richards fig. 12: within PLL output of Z^-1 including 1216, 1218, 1220, 1222, and DPLL indicated inside 1208) within said PLL by way of said control signal (see quote above in Richards).

30. As per claim 18, the method of claim 17, wherein said altering comprises at least one of engaging and disengaging (Richards fig. 12: in PLL, wipe-off registers A&B occurs send control signals to mux at certain points which effectively engages or disengages the mux) at least one circuit element into said feedback loop in response to said control signal.

31. As per claim 19, the method of claim 16, further comprising switching another clock source to said input of said PLL in response to said control signal. (Richards fig. 12: within 1208, the bit-sync control effectively switches another clock source in order to synchronize. Bit-synch control is receiving a control signal from the bottom)

32. As per claim 20, the method of claim 19, wherein said switching to said other clock source includes switching from a bus received clock source to a local clock source (Richards fig. 12: bit sync control is looking to see if a bit is not in sync (i.e. the bit is affected by another clock) then it will change the bit synchronization via its locally determined synchronization which inherently uses its local clock since that is the only clock the bit synchronizer has.).

33. Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

35. A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

36. Claims 5, 6, 8, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bedrosian.

37. As per claim 5, the circuit of claim 4, wherein said at least one circuit element includes a capacitor in parallel with said resistor (not in Bedrosian; however, the selection of known material based on its suitability for the intended use for prior art parts does not make the claimed invention patentable over that prior art (In re Leshin, 125 USPQ 416).).

38. As per claim 6, the circuit of claim 2, wherein said feedforward circuitry includes at least one of a resistor and a capacitor in parallel with said switch (not in Bedrosian; however, the

selection of known material based on its suitability for the intended use for prior art parts does not make the claimed invention patentable over that prior art (In re Leshin, 125 USPQ 416).).

39. As per claim 8, the circuit of claim 7, wherein said bias network includes a resistor based voltage divider. (not in Bedrosian; however, the selection of known material based on its suitability for the intended use for prior art parts does not make the claimed invention patentable over that prior art (In re Leshin, 125 USPQ 416).).

40. As per claim 9, the circuit of claim 8, further including a zener diode in parallel with at least one resistor of said resistor base voltage divider. (not in Bedrosian; however, the selection of known material based on its suitability for the intended use for prior art parts does not make the claimed invention patentable over that prior art (In re Leshin, 125 USPQ 416).).

41. Conclusion

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on Monday through Thursday after 8AM to after 6:30PM.

43. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on (703) 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

44. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

45. 46.

47. PK
48. October 7, 2002

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 10/10/02